

REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the subject application. The Advisory Action dated May 29, 2003 and the Final Office Action of January 13, 2003 has been received and contents carefully reviewed.

In the Final Office Action, the Examiner rejected claims 33-47, 64-66, and 68-71 under 35 U.S.C. § 103(a) as being unpatentable over the related art shown in Figures 1a and 1b in view of Hebiguchi (U.S. Pat. No. 6,091,473, hereinafter referred to as 'Hebiguchi '473'); rejected claims 48-60, 62, and 63 under 35 U.S.C. § 103(a) as being unpatentable over the related art shown in Figures 1a and 1b in view of Hebiguchi (U.S. Pat. No. 6,137,557, hereinafter referred to as 'Hebiguchi '557'); rejected claim 61 under 35 U.S.C. § 103(a) as being unpatentable over the related art shown in Figures 1a and 1b in view of Hebiguchi '557 and further in view of Hebiguchi '473; and objected to claim 67 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant submits that the rejections set forth in the Final Office Action are moot in view of the amendments set forth herein. Reconsideration of the claims is respectfully requested in view of the foregoing amendments to the claims and the following remarks.

The Examiner is thanked for the indication of allowable subject matter in claim 67. Applicant have amended claim 67 to be in independent form incorporating the limitations of the base claims and any intervening claims. Therefore, Applicant submits that this claim is in condition for allowance.

With respect to independent claim 33, claim 33 and claims 34-47, which ultimately depend therefrom, are allowable over the cited references in that each of these claim recites at least "the data electrodes including a first capacitor portion overlapping the common line and

the common electrodes including a second capacitor portion overlapping the common line, the first and second capacitor portions substantially parallel to the gate bus line.” None of the cited references, either singly or in combination, teaches or suggests at least these features of the claimed invention. Therefore, Applicant submits that claim 33, and claims 34-47, which depend therefrom, are allowable over the cited references.

With respect to independent claim 48, claim 48 and claims 49-63, which ultimately depend therefrom, are allowable over the cited references in that each of these claim recites at least “data electrodes parallel to the data bus line in the pixel region, common electrodes including parallel portions substantially parallel to the data bus line and a connecting portion substantially parallel to the gate bus line, the parallel portions extending from the connecting portion and having an oblique side.” None of the cited references, either singly or in combination, teaches or suggests at least these features of the claimed invention. Therefore, Applicant submits that claim 48, and claims 49-63, which depend therefrom, are allowable over the cited references.

With respect to independent claim 64, claim 64 and claims 65-66 and 68, which ultimately depend therefrom, are allowable over the cited references in that each of these claim recites at least “data and common electrodes parallel to the data bus line in the pixel region, the data electrodes including a first capacitor portion overlapping the common line and the common electrodes including a second capacitor portion overlapping the common line, the first and second capacitor portions substantially parallel to the gate bus line.” None of the cited references, either singly or in combination, teaches or suggests at least these

features of the claimed invention. Therefore, Applicant submits that claim 64, and claims 65-66 and 68, which depend therefrom, are allowable over the cited references.

With respect to independent claim 69, claim 69 and claims 70-71, which ultimately depend therefrom, are allowable over the cited references in that each of these claim recites at least "data and common electrodes parallel to the data bus line in the pixel region, the data electrodes including a first capacitor portion overlapping the common line and the common electrodes including a second capacitor portion overlapping the common line, the first and second capacitor portions substantially parallel to the gate bus line." None of the cited references, either singly or in combination, teaches or suggests at least these features of the claimed invention. Therefore, Applicant submits that claim 69, and claims 70-71, which depend therefrom, are allowable over the cited references.

Should the Examiner deem that a telephone conference would further the prosecution of this application, the Examiner is invited to call the undersigned attorney at (202) 496-7500.

Application No.: 10/015,765
Group Art Unit: 2871

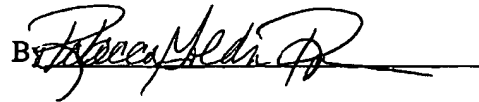
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The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 50-0911, under Order No. 8733.250.21.00-US. A duplicate copy of this paper is enclosed.

Respectfully submitted,

McKENNA LONG & ALDRIDGE LLP

Date: October 14, 2003

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